

CHARACTERISTICS OF TRENCHED COPLANAR WAVEGUIDE FOR SiMMIC APPLICATIONS

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ABSTRACT

A novel low loss trenched aluminium CPW transmission line structure, fabricated on a selection of high, medium and low resistivity silicon substrate materials, is reported. In comparison with conventional aluminium conductor CPW line structures, RF losses are reduced. For 10 K Ω cm high resistivity material, this reduction may be as much as 0.5 dB/cm at 30 GHz, achieved by etching longitudinal trenches in the silicon substrate material. For medium resistivity substrates (700 - 1000 Ω cm,) a 13 μ m deep trench reduces measured line loss from 3.9 dB/cm to 3.4 dB/cm at 30 GHz. For low resistivity silicon substrate material (10-20 Ω cm), RF losses can be improved by 36 dB/cm at 30 GHz with 80 μ m deep trenches. The effect of the trench depth on the characteristic impedance of these CPW lines is reported.

INTRODUCTION

Losses in conventional CPW lines, Figure 1 (a), on medium (700-1000 Ω .cm) and low (10-20 Ω .cm) resistivity silicon substrates are mainly contributed by conductor loss, ohmic loss within the dielectric material and dielectric loss^[1,2]. In high resistivity silicon substrates (>2 K Ω .cm) these losses are dominated in the microwave

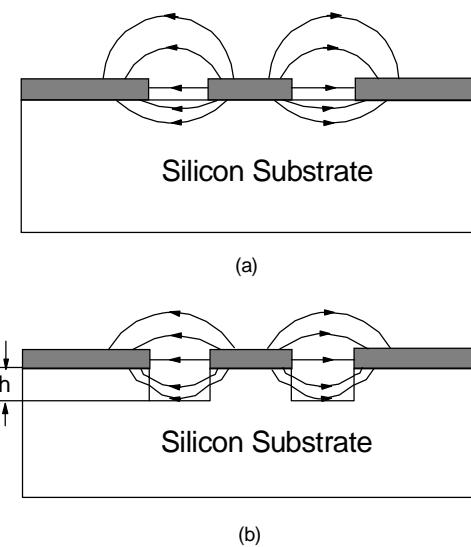


Figure 1 Coplanar Waveguide
(a) Conventional Structure
(b) Trenched Structure

frequency range by conductor loss^[1, 3-5]. The amount of conductor loss is not only determined by the conductivity of the conductor, but also the distribution of current on the signal and ground conductors^[6]. Current crowding at the edges of the signal and ground lines results in high conductor loss which intensifies when the dielectric constant of the substrate increases^[7]. By lowering the dielectric constant of the substrate at the edges of the strip and ground conductors, current crowding at the edges can be reduced and hence conductor loss reduced. A CPW line embodying this concept is illustrated in Figure 1 (b). The figure shows that the trench pairs introduced between signal and ground lines

lower the apparent dielectric constant in the region through which the majority of electromagnetic field energy propagates. This trench arrangement effectively reduces the current densities at the edges and results in lower conductor loss. Furthermore, for low and medium resistivity silicon substrates, the presence of the trenches reduce ohmic loss within the dielectric. For trenched CPW line, this effect is much more marked than for etched microstrip line^[7].

TRENCHED CPW LINES

Trench etched CPW transmission lines have been fabricated on (i) 650 μm thick, 5-10 $\text{K}\Omega\text{.cm}$ resistivity silicon substrates, (ii) 380 μm thick, 700-1000 $\text{K}\Omega\text{.cm}$ medium resistivity silicon substrates and (iii) 560 μm thick, 10-20 $\Omega\text{.cm}$ low resistivity silicon substrates, each with $<100>$ crystal orientation. Conductor metallization is formed using evaporated aluminium of thickness 1.46 μm for the high resistivity case, 1.0 μm for the low resistivity substrates, while 0.3 μm evaporated aluminium metallization is used for the medium resistivity case. The signal line width is 70 μm , and the gap between signal and ground lines is 40 μm for all the cases. The trenches are realised using a CF_4 plasma etch. The silicon etch rate is about 1.5 μm per hour with 70 W RF power and 150 mTorr pressure. Figure 5 shows a micrograph of a 10 μm deep trench in the medium resistivity case.

The lines were measured using an HP 8510B network Analyser and Cascade wafer probe station with 200 μm G.S.G. coplanar probes, calibrated using LRM to the probe tips, taking care to eliminate reflection losses^[5].

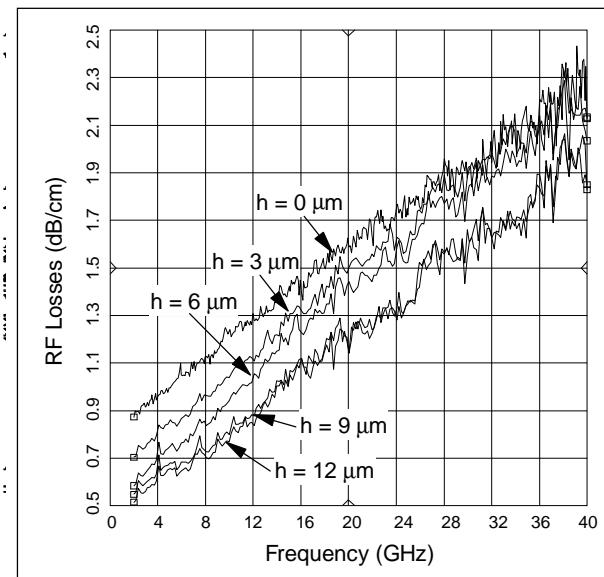


Figure 2 The measured RF losses of CPW lines on high resistivity silicon substrate with zero, 3 μm , 6 μm , 9 μm and 12 μm deep trenches

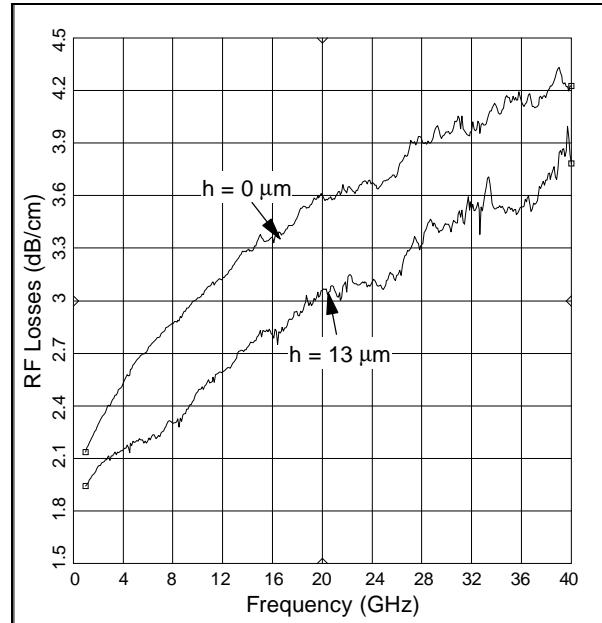


Figure 3 The measured RF losses of CPW lines on medium resistivity silicon substrate with zero and 13 μm deep trenches

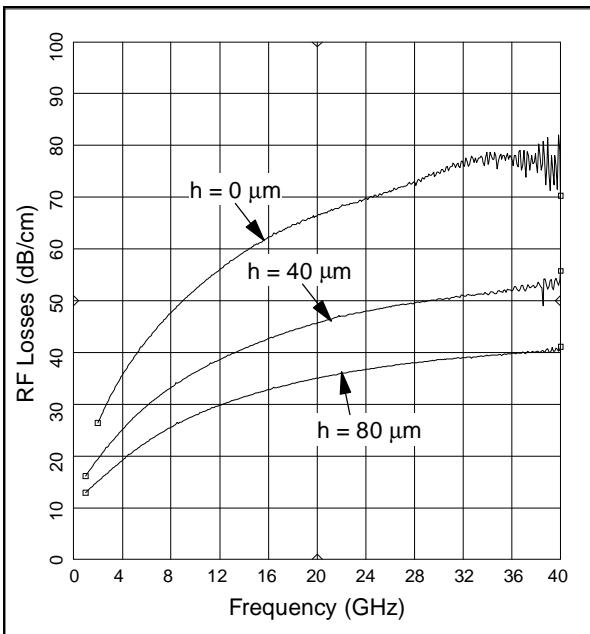


Figure 4 The Measured RF losses of CPW lines on low resistivity silicon substrate with zero, 40 μ m and 80 μ m deep trenches

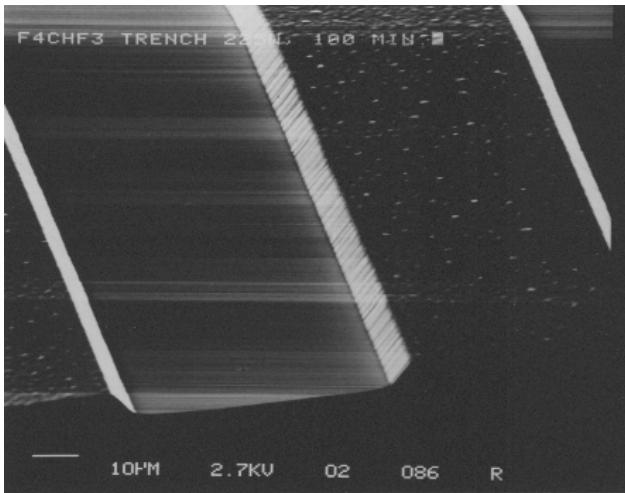


Figure 5 Microphotograph of a 10 μ m trenched CPW line on medium resistivity silicon substrate

RESULTS

The measured RF losses for zero to 12 μ m deep trenches, etched in CPW lines on the high resistivity silicon substrate, are illustrated in Figure 2. As can be seen, without trenches, RF losses are 1.2 dB/cm at 10 GHz and 1.9 dB/cm at 30 GHz. With 9 μ m deep trenches, the line dissipation losses are reduced to 0.8 dB/cm at 10 GHz and 1.6 dB/cm at 30 GHz.

Figure 3 illustrates the RF losses on the medium resistivity silicon substrate. With 13 μ m deep trenches, the average RF losses from 1 to 40 GHz have improved by about 0.5 dB/cm. Figure 4 shows the RF losses on the low resistivity silicon substrate. As can be seen, the RF losses have been reduced by 23 dB/cm at 10 GHz and 36 dB/cm at 30 GHz respectively, with 80 μ m deep trenches, when compared to the unetched case.

As the lines are etched, the equivalent dielectric constant presented to the propagating wave also changes. This results in a variation of characteristic impedance. The input impedance of the trench lines, from which the line characteristic impedance is inferred, in all cases increases with trench depth, eg. in the high resistivity case, the inferred Z_0 changes from 55 ohm to 60 ohm as trench depth varies from 0 to 9 μ m.

CONCLUSIONS

The characteristics of trenched coplanar waveguide for SiMMIC applications have been established for the first time. By introducing trench etched CPW lines, current crowding at the edges of signal and ground lines can be reduced and, hence, lower effective conductor loss is observed. In all cases measured, loss reduces with increasing trench depth, the effect

being most significant with lower resistivity substrates

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REFERENCES

- [1] A. Rosen et al., "Silicon as a millimetre-wave monolithically integrated substrate - a new look", *RCA Review*, 1981, Vol. 42, pp. 633-660.
- [2] K.C. Gupta et al., "Microstrip lines and slotlines", 2nd ed., Artech House, Boston, 1996.
- [3] J. Beuchler et al., "Silicon high-resistivity-substrate millimetre-wave technology", *IEEE Trans. Microwave Theory Tech.*, Vol. 34, pp. 1516-1521, Dec. 1986.
- [4] S.R. Taub and P. Young, "Temperature dependent performance of coplanar waveguide (CPW) on substrates of various materials", *IEEE MTT-S Digest*, pp. 1049-1051, 1994.
- [5] V.F. Fusco et al., "Silicon interconnect for millimetre wave circuits", *Proceeding of 25th European Microwave Conference*, pp. 467-469, Sep. 1995.
- [6] D. Budimir et al., "Low loss multilayer coplanar waveguide transmission lines on silicon substrate for MMICs", *Proceeding of 26th European Microwave Conference*, pp. 697-700, Sep. 1996.
- [7] K. Li and K. Atsuki, "Low conductor loss microstrip lines with side-grooves", *IEEE MTT-S Digest*, pp. 311-314, June 1996.